ABSTRACT OF THE DISCLOSURE

The bottom side of an N type silicon substrate is connected to a power supply terminal, a second P type epitaxial layer is formed on all sides of the N type silicon substrate, and a device forming portion is provided on the second P type epitaxial layer. A first P type epitaxial layer and an interlayer insulating film are provided on the device forming portion and an N well and a P well are formed on the top surface of the first P type epitaxial layer. The second P type epitaxial layer is connected to a ground terminal via the first P type epitaxial layer, the P well, a p^+ diffusion region, a via and a wire. Accordingly, a pn junction is formed at the interface between the second P type epitaxial layer and the N type silicon substrate.